AMENDMENTS TO THE ABSTRACT

Please amend the abstract at paragraph 0092 as follows:

[0092] A field-programmable gate array (FPGA) ~~comprising~~ having an array of RAM memory cells comprising at least one row of RAM memory cells, each RAM cell of the at least one row of RAM memory cells coupled to a row driver line; a row decoder coupled to a first end of the row driver line of each at least one row of RAM memory cells.~~; a~~ A monitoring memory cell is coupled to ~~at least one of the~~ a row driver line. ~~; and where each~~ Each monitoring memory cell is also coupled to a memory writing line. ~~A method for an~~ An FPGA ~~having a plurality of~~ also has RAM memory cells that act as the programming mechanism.[,] ~~the~~ The FPGA further ~~having~~ has erase circuitry for clearing the RAM memory cells for reprogramming of the FPGA. The ~~method comprises~~ FPGA is erased by providing at least one monitoring memory cell coupled to the erase circuitry.[;] ~~initiating a~~ A memory clear phase is initiated on at least one monitoring memory cell. ~~; and making a determination as to whether the output signal from each at least one monitoring memory cell indicates a cleared monitoring memory cell~~. The monitoring memory cell then indicts the cell has been cleared. ~~The method may further comprise an act of writing to the at least one monitoring memory cell and a query of determining whether all of the at least one monitoring cell was properly written to.~~